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A VERY LOW ENERGY ELECTROSTATIC ANALYZER,(U)

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A VERY LOW ENERGY ELECTROSTATIC ANALYZER

ROBERT E. LA QUEY

Maya Development Corporation
11675 "H" Sorrento Valley Road
San Diego, California 92121

Scientific Report No. 1

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An electrostatic analyzer is described that can be applied to obtaining the differential energy spectrum of very low energy ions or electrons in the energy range 1 to 100 eV. This instrument is designed to operate at magnetic field strengths up to 0.5 gauss and is adaptable to construction as an array of sensing elements.

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CONTENTS

SUMMARY

In this report we describe an instrument development program which has been conducted for the Air Force Geophysics Laboratory by MAYA Development Corporation. The goal of this program is the design of very low energy particle differential analyzer for the energy range of 0.1 ev to 1.0 ev.

An artists conception of the resulting instrument is shown in Figure 1. The cylindrical structure contains a super array of Flat Plate Microanalyzer Arrays (FPMA's) which are described in detail in the body of this report. A spiraltron supported by its holder is shown in cutaway section. The spiraltron acts as a detector of electrons or protons which have been analyzed by the FPMA's. The supporting box contains the high voltage electronics, amplifiers, and microprocessor based control circuitry which are required to operate the instrument.

Hardware consisting of a spiraltron, with holder, preamplifier and high voltage supply is delivered with this report.

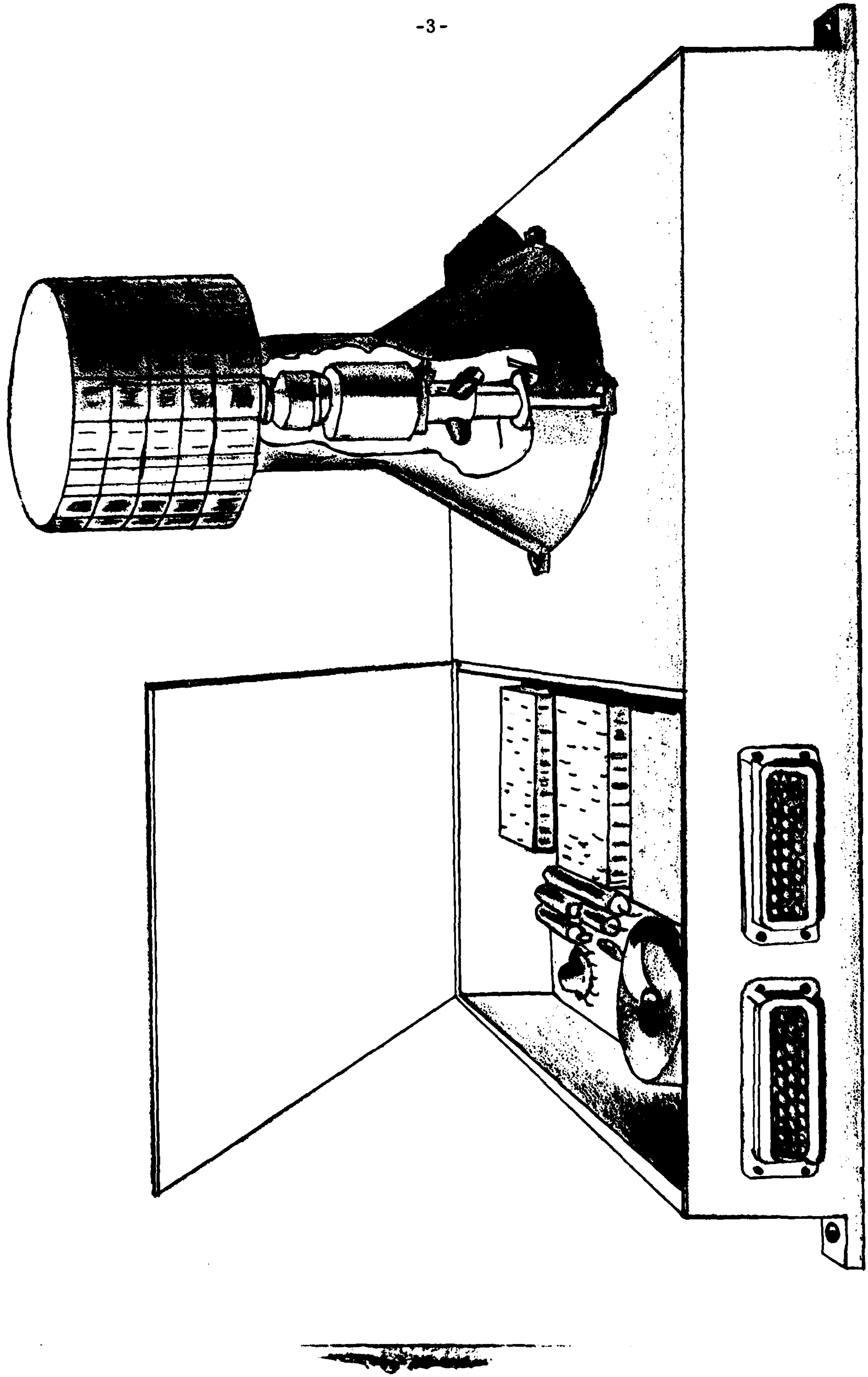
INTRODUCTION

The magnetic field in low earth orbit is approximately 0.3 gauss in magnitude. In a satellite that is not oriented with respect to the magnetic field (the most common case) this field must be considered as an extreme complication to the problem of measuring low energy electrons. In Table 1, we present the electron cyclotron radius for low energy electrons orbiting in various field strengths.

B, V=10^{-5} Gauss	3×10^4	3×10^3	3×10^2
W ev	r cm	r cm	r cm
1	11.2	112	1,120
.1	3.5	35	350
.01	1.12	11.2	112

TABLE 1

The advanced Technology Satellite Auroral Particles Detectors and the UCSD instrument on SCATHA are operating at geosynchronous orbit, where the magnetic field is typically of order 100 γ. The electron gyroradius is no problem in these instruments. But for a low energy analyzer in near earth orbit the situation is very different. At 0.1 ev the cyclotron radius is comparable to the size (electron) of the instrument and would introduce a major error into the measurement. The effect of the gyroradius on low energy electron instruments must be a matter of primary concern.



A simple parameter $\varepsilon = \frac{R}{r}$ characterizes the magnitude of the problem for various detectors. Here R is the scale size of the orbit in the instrument with no magnetic field and r is the electron gyroradius. For a cylindrical analyzer

$$\varepsilon = \frac{R}{r} = \frac{2\ W}{MeC^2}^{1/2} \frac{dB}{V}$$

where W = particle energy
MeC^2 = electron rest mass energy
d = plate separation
V = plate voltage
B = magnetic field .

One must require $\varepsilon \ll 1$ or the instrument will be strongly affected by the magnetic field.

After much thought a number of techniques for the nulling out of the magnetic field have been discarded as not feasible. Instead, we believe that the design of a low energy differential analyzer must be insensitive to the magnetic field at whatever orbit it is intended to operate.

To attain this goal, the design of a low energy differential analyzer which is insensitive to the magnetic field, we have developed an innovative approach which emphasizes miniaturization of the analyzer. Thus we seek to design an analyzer for which $R \ll r$ so that the magnetic field corrections to particle orbits through the analyzer are negligible.

Once one decides to miniaturize an analyzer two problems immediately present themselves: 1) How does one fabricate the analyzer? 2) How does one overcome the inherently small geometric factor implicit in a miniature analyzer. The answer to the first question fortunately suggests a means of solving the second. The fabrication technique which we explore in this report is based upon modern ceramics technology as practiced in the manufacture of thick film hybrid circuits and as utilized

by the capacitor industry. The techniques we shall develop are mass production techniques which suggest that the miniature analyzers we are designing should be produced in large numbers. Thus, by using these analyzers in arrays the limitation on geometric factor can be overcome.

In order to simplify the fabrication and analysis of the microanalyzer we have chosen initially to focus upon a very simple flat plate design. These flat plates will be arrayed in a structure we call a Flat Plate Microanalyzer Array (FPMA).

Finally, we note that the technical environment in which these new detectors are being developed is very much different from that in which earlier designs such as the ATS and SCATHA instruments were developed. The basic designs for the analyzers on board the ATS and SCATHA were developed almost a decade ago. The very rapid advance in semiconductor technology, in particular the development of Large Scale Integration (LSI) of microelectronic circuitry, opens up new vistas for the realization of a new generation of "smart" instruments. These instruments will provide new physical data previously unobtainable and will also act as test beds for the development of LSI techniques in electronic systems in space which will have implications for the major missions of the USAF throughout the next decade.

The electronics which supports the implementation of a Flat Plate Microanalyzer Array will rely heavily upon these advances in LSI. Indeed, the implementation of an instrument based upon the FPMA would not have been practical prior to the advent of the microprocessor.

THE FLAT PLATE MICROANALYZER ARRAY

During this reporting period we have begun a detailed examination of the problems of miniaturization and of production of arrays of analyzers. We are happy to report optimistic results of this investigation. It appears that existing techniques that have been highly developed for the construction of hybrid circuits and for the interconnection of Large Scale Integrated (LSI) circuitry can be applied to the problem of analyzer miniaturization. A fruitful cross-fertilization of LSI techniques with analyzer design problems is resulting. The decision to miniaturize analyzers, while providing a direction for this effort, still leaves many questions unresolved. Particularly pressing is the question, "What shape should the plates be?" Without elaborating on all of the reasons, we have chosen a very simple approach, the flat plate analyzers.

Among the advantages of a flat plate analyzer are the following:

1) Simplicity of construction, and hence a reasonable chance at miniaturization.

2) Plates may be positioned out of the line of sight of both high energy particles and photons, thus secondary electrons produced within the analyzer can be minimized.

3) The analyzer constant is small, which is an advantage at low energies.

4. A simple analytic model is available for preliminary analysis of the particle orbits.

Disadvantages in the form of poor energy and angular response exist, but the clever use of arrays may improve on these.

A brief discussion of the fabrication techniques is in order. Details are difficult to describe in writing without constant reference to prints, but the basic idea can be presented. The plates will be printed using standard photo lithographic techniques on ceramic substrates. A box will be assembled (by soldering or brazing) these parts together. Collimators can be constructed by similar techniques. The entire assembly is put together much like a child would build a house of cards and blocks, except it is much smaller. The basic parts will be quite highly precise dimensionally and will form building blocks for the construction of a wide variety of miniature analyzers. Our initial design goal is 10 flat plate analyzers with collimators in a 1 cm cube. Consultations with experts in the field of ceramic interconnection technology indicate that these goals, while radical from the perspective of the instrument designer, are almost conservative to the point of boredom for the ceramics specialists. We hope by applying a new technique to an old problem to achieve a true breakthrough in electrostatic analyzer design.

As the design proceeds, we shall determine what the limits of miniaturization are and how increasing miniaturization effects the unit costs. By such a proceeding we anticipate a final unit which has the unique properties of low unit cost and ease of replication. Existing analyzers all suffer from the "prototype" syndrome. Namely, they are designed to be produced one at a time by detailed and old-fashioned hand machining techniques. The resulting analyzers are quite expensive, are large, and cannot be considered for use in arrays, thus failing to exploit one of the primary facts of modern LSI technology, the inexpensive electronic expansion of control capabilities. Thus by designing a set of basic building blocks for Flat Plate Microanalyzer Arrays (FPMA), we have the fundametal module needed for the next generation of instruments.

Note also that this technique is one that is prevalent in the

fabrication of hybrid circuitry and can be applied to the interconnection of LSI components. Thus while one is developing the technique for the FPMA, one also develops as spin off a powerful electronics assembly technique that will enrich a broad spectrum of USAF programs.

Finally, we note that while design objectives in the 0.1 ev to 1 ev range remain in force, the FPMA will be examined with the idea of including the energy range from 1 ev to 100 ev in its capability. Indeed this energy range probably results naturally from simply increasing the plate voltages, and high performance is almost certainly more easily attainable in this energy range.

TRAJECTORY ANALYSIS

As an introduction to the Flat Plate Microanalyzer Array we have performed the preliminary trajectory analysis of a single analyzer in the FPMA. The analyzer does not have particularly impressive focusing properties, but we would argue that when used in an array the focusing properties of an individual analyzer become less important than the focusing properties of the array as a whole. And, as with antenna arrays, the focusing properties of an analyzer array can be better than that of an individual analyzer.

A summary is presented herein of the results of the trajectory analysis.

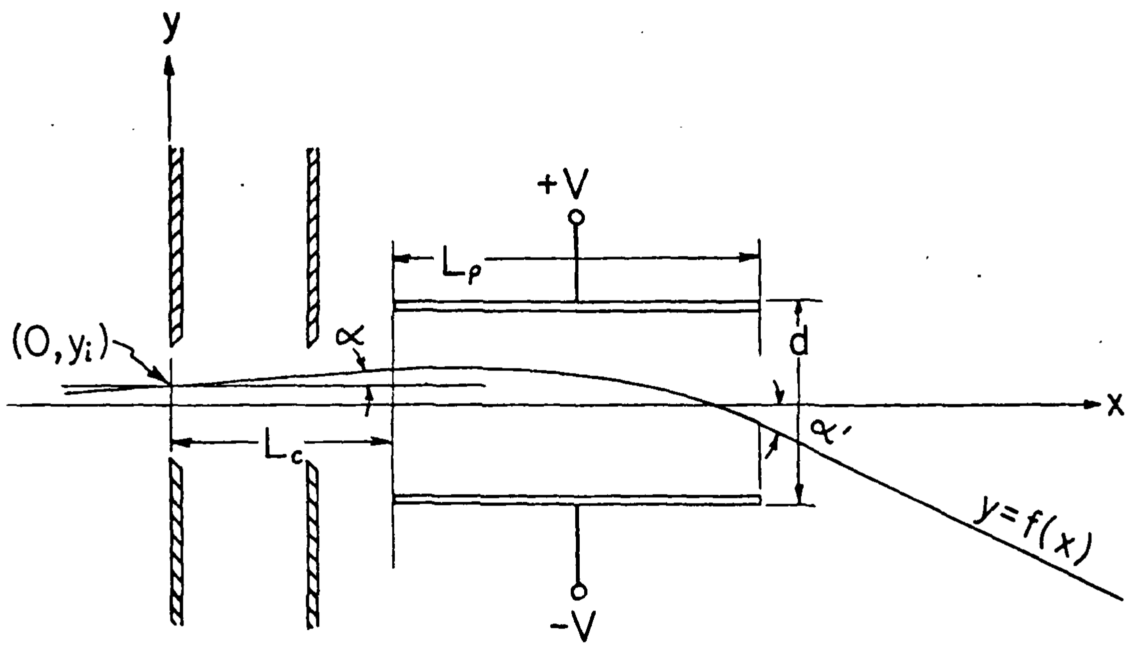


Figure 1

Referring to Figure 1, we find the following results for trajectories through an individual flat plate analyzer.

Given ε = particle kinetic energy = $\frac{1}{2}mv^2$, α = particle entrance angle, and y_i = initial displacement from the central axis of teh analyzer then

$$y = y_i + x\tan\alpha - [x-(L_p+L_c)]\left(\frac{eV}{\varepsilon}\right)\left(\frac{L_p}{d}\right)\frac{1}{\cos^2\alpha} - \frac{1}{2}\left(\frac{eV}{\varepsilon}\right)\left(\frac{L_p}{d}\right)L_p\frac{1}{\cos^2\alpha}$$

Where

Lp = plate length

Lc = distance from apperture to the front of the plates

d = plate separation

V = potential applied to each plate

Now for small entrance angles one can write this as

$$\Delta y = y - y_i = \left(\frac{eV}{\varepsilon}\right)\left(\frac{L_p}{d}\right)\left(x - \frac{1}{2}L_p - L_c\right)(1+\alpha^2) + x\alpha$$

Thus we see that there is a linear term in α which prevents focusing and is hence undesirable. The term springs from the tan α in the full expression, and is not easily eliminated in this geometry. The best we can do is demand that $\left(\frac{eV}{\varepsilon}\right)\left(\frac{L_p}{d}\right) \gg \alpha$ so that the linear term is swamped by the zero order terms. Thus we require that the angular deflection imposed by the analyzer is large compared to the allowable entrance angles. This does <u>not</u> cause the analyzer to focus, but it does limit the negative consequences of the lack of focus.

The key design equation is the one describing the angular deflection

$$\tan \alpha' = \tan \alpha - \left(\frac{eV}{\varepsilon}\right)\left(\frac{L_p}{d}\right)\left(\frac{1}{\cos^2\alpha}\right)$$

Defining $\Delta\alpha = \alpha - \alpha'$ and performing some algebra one finds that

$$\Delta\alpha \simeq -\epsilon\,(1+\epsilon\alpha)$$

Where

$$\epsilon \equiv \left(\frac{eV}{\mathcal{E}}\right)\left(\frac{L_p}{d}\right)$$

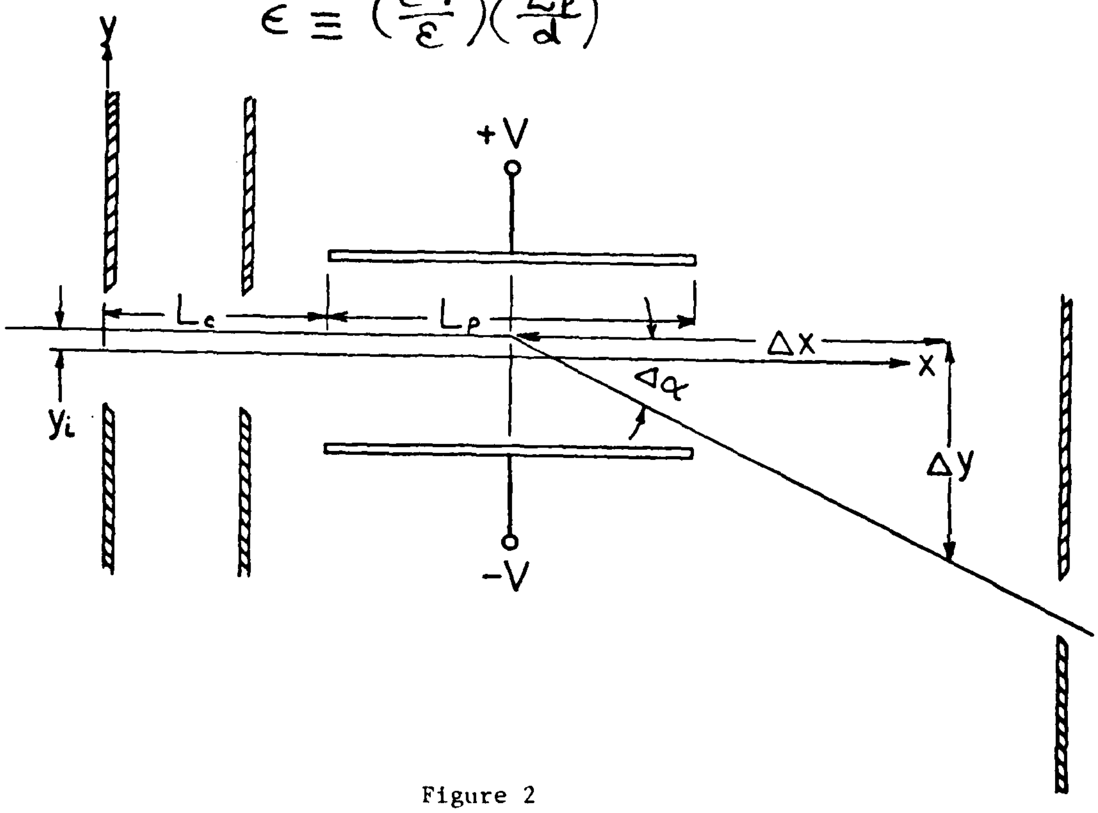


Figure 2

Now referring to Figure 2 we have

$$\Delta y = \Delta\alpha\,\Delta x$$

Where

$$\Delta y = y - y_i$$
$$\Delta x = x - L_c - \tfrac{1}{2} L_p$$
$$\Delta\alpha \simeq -\epsilon$$ in lowest approximation.

In the design we will fix Δy and Δx by the placement of an exit apperture then

$$\epsilon = -\left(\frac{\Delta y}{\Delta x}\right)$$

will define the accepted energies. Alternatively, if the apperture is a slit, then the collimator will define the energy resolution.

FABRICATION TECHNIQUE

The fabrication technique for the FPMA is as follows:

1. Using castable alumina and a metal mold, a section with a cross-section as shown in Fig. A would be cast 3 inches long.

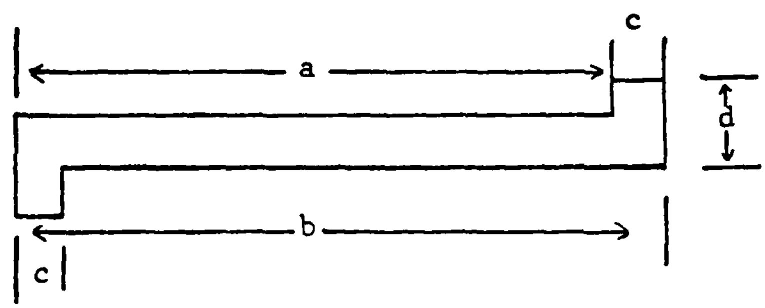


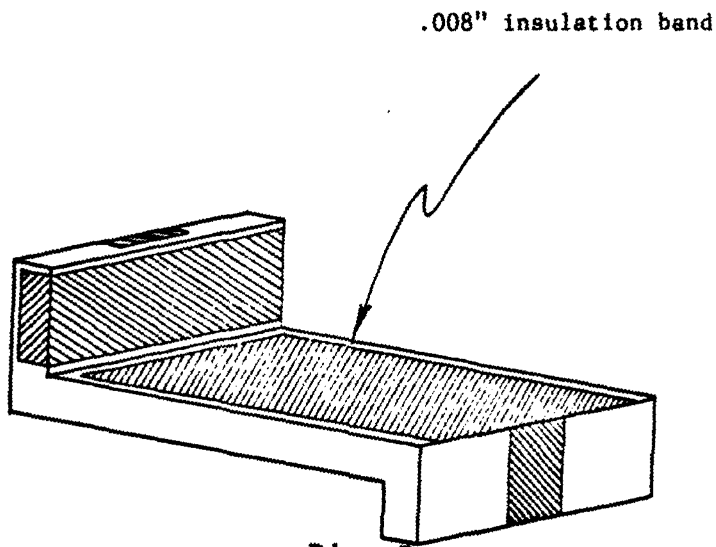
Fig. A

2. The binder formulation for the alumina would be designed to allow knife cutting in the green state. This would allow the 3 inch section to be cut into appropriate sections by being clamped in a simple holding fixture and cut with a razor blade.

3. *The section would be fired.*

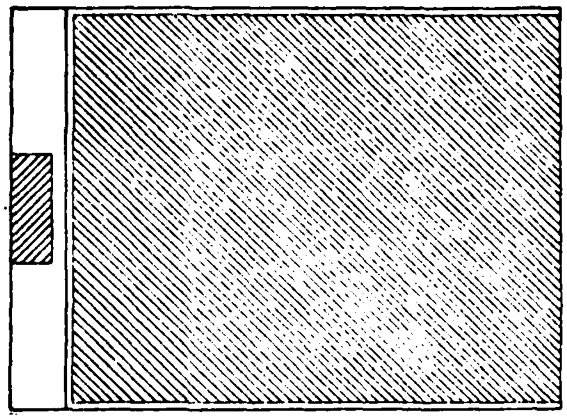
4. Silver or gold metalization as required would be applied by hand with a brush or similar instrument and metalic/glass frit ink while parts are held by tweezers. The internal corners could be inked and, when dry, an insu-

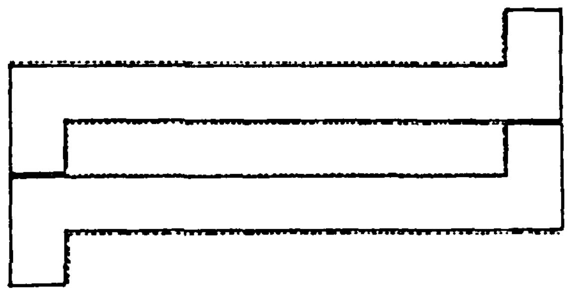
lation strip could be scratched through with a pointed instrument. Metalization would be semetrical from top to bottom as shown in Dia. B.

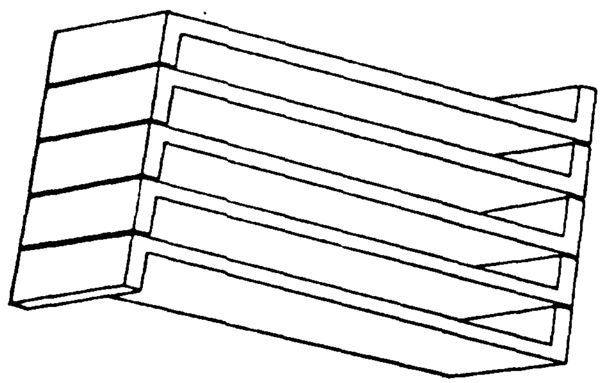


Dia. B.

5. After initial metalization, parts would be low temp pre-fired to partially fuse frit, and remove volatile vehicle constituents from metalic ink.







Alternate Ceramic Formation

1. Using saurhizen compound, which is a castable ceramic material that does not require firing and can withstand moderate temperatures. It offers the advantage over fired systems of dimensional stability -- absence of shrinkage during firing.

2. Using saurhizen compound, the individual parts would be cast in a silicone mold.

Should these techniques be applied to a mass spectrometer, then we would need to extend our examination to include magnetic ceramics. Here again, a large and well known technology exists based upon the ferrite group (Fe_2O_3). These ceramic materials are characterized by high electrical resistivity, modest remanence, and high coercivity. Again, by emphasizing casting and production oriented techniques, we would hope to make the individual analyzers inexpensive enough so as to produce arrays of them. This may, indeed, be the only way to ultimately achieve geometry factors that are large enough to produce significant high-time resolution studies of magnetosphere ion dynamics. Our emphasis here would be less upon miniaturization than upon mass production of precision parts using ceramic casting and forming techniques. The end result would be low-cost precision analyzers as demanded for array use.

CALIBRATION

There are two major problems, which must be solved in order to calibrate an FPMA. First, there are the problems associated with the very low energies of the particles we wish to analyze. The energy range of 0.1 ev to 1.0 ev requires extreme attention to detail. The test facility must be very well shielded and all contact potentials must be properly understood. There are however no problems of a fundamental nature to be overcome.

The use of arrays with the implication that many analyzers must be calibrated presents another problem. Old fashioned manual data taking must be replaced with a greater degree of automation because of the repetitive nature of the testing required. Fortunately advances in microcomputer technology make the required Instrument Development and Support System (IDSS) a viable and cost effective undertaking. A microcomputer based IDSS (See Section 5) will be specified as the instrument design evolves toward completion.

THE INSTRUMENT ELECTRONICS

Preliminary definition of the electronics to be used with the Flat Plate Microanalyzer Array (FPMA) has begun. Ultimately, instruments will be built which employ many FPMA's in larger arrays. As an example, we consider the implementation of the electronic controller for a rectangular array of FPMA's. Each FPMA would be an element in this array. The array would be programmed by using an onboard microprocessor, to map out the desired analog voltages represented digitally in the microprocessor memory onto the individual plates of each FPMA. (See Figure 1)

A block diagram of the microprocessor-based controller is indicated in Figure 2. A control program located in the PROM would define the instrument operation. This program would perform the following functions:

1) Scan and read telemetry commands into RAM.

2) Interpret commands, set up break points, and enter data into control programs.

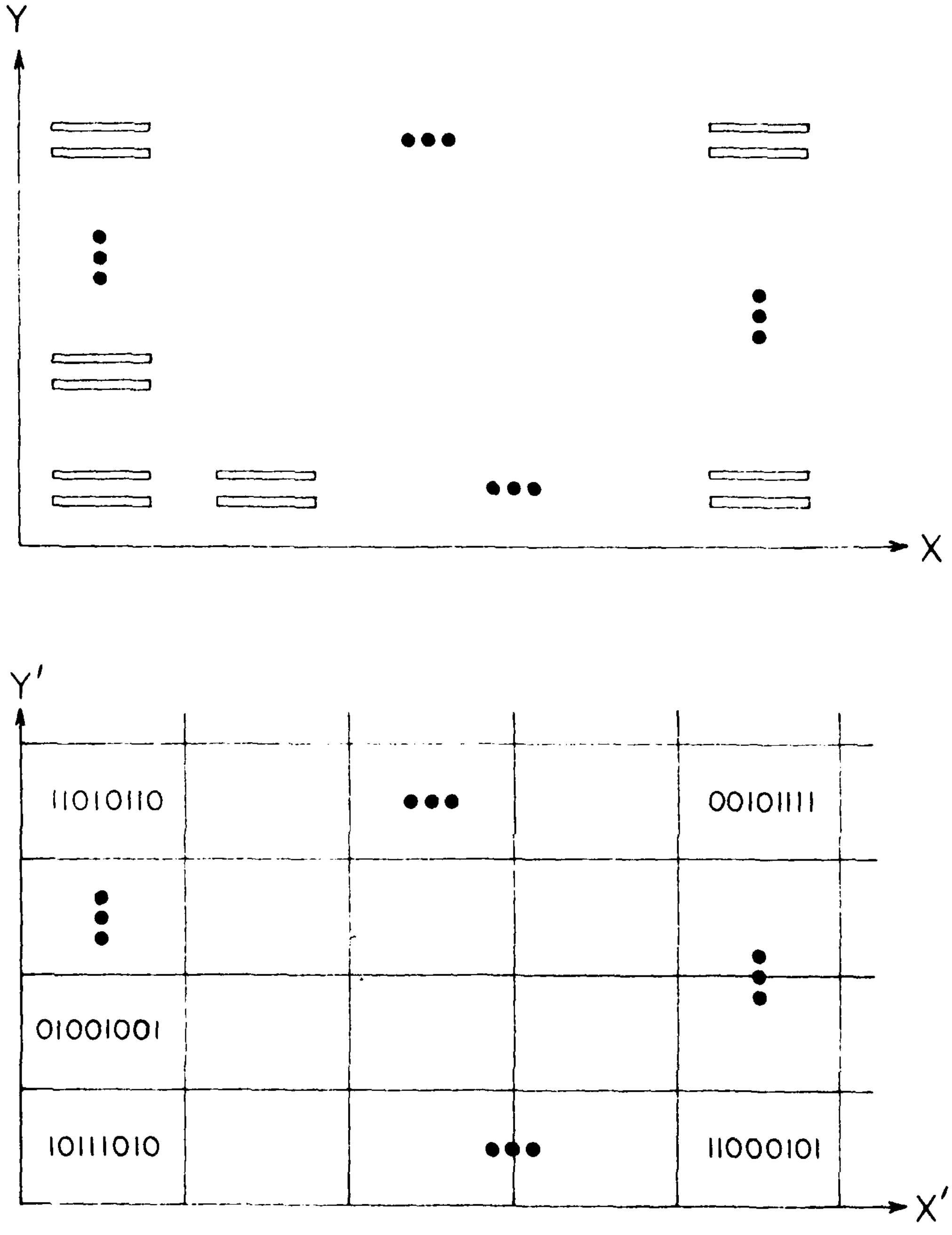
3) Read into RAM the Most Significant Bits (MSB's) and Least Significant Bits (LSB's) of the detector pulse counter.

4) Format data from the detector pulse counter.

5) Read data from RAM out to the telemetry interface.

6) Execute FPMA scan programs.

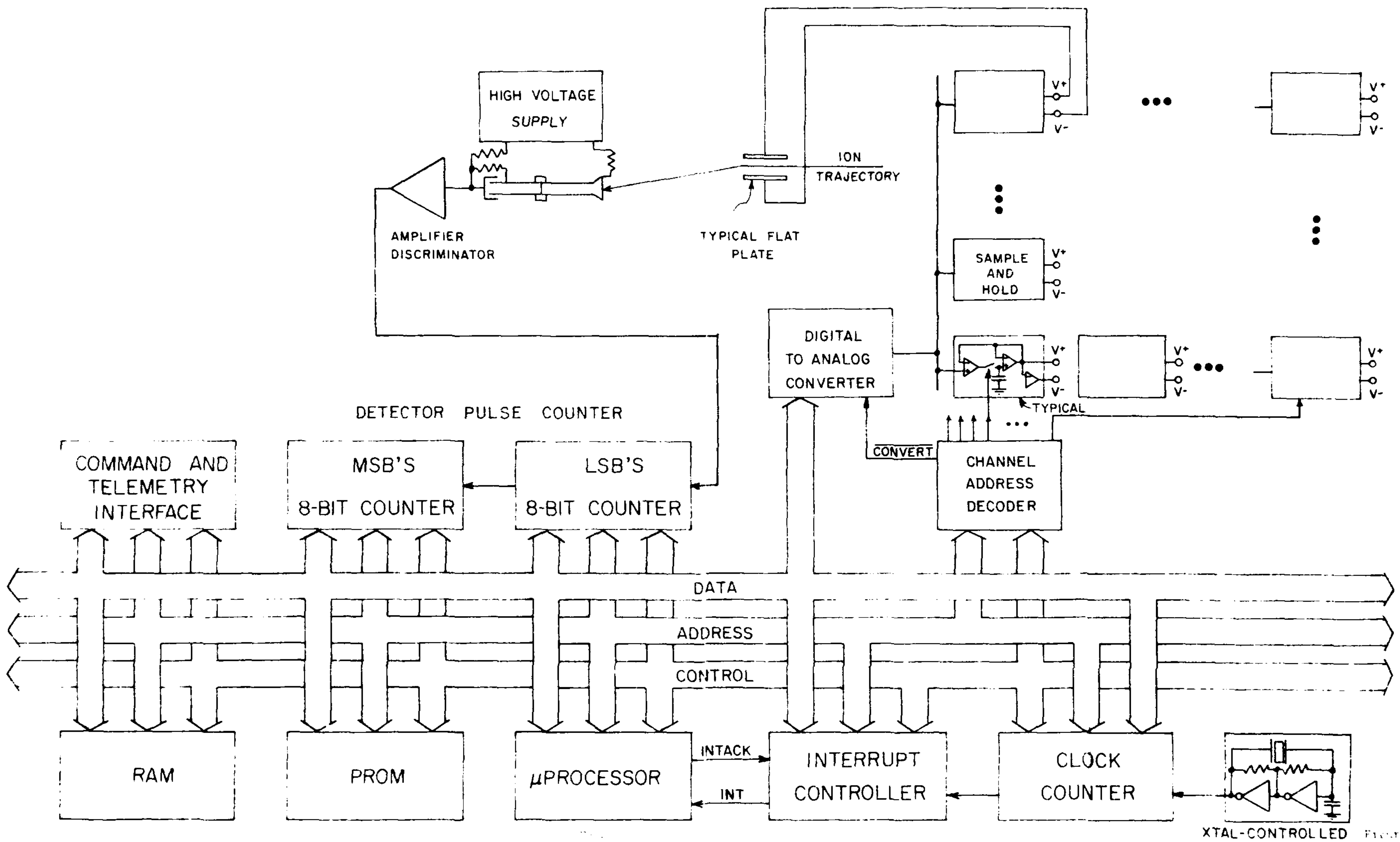
7) Perform system diagnostics and gather housekeeping data.



MEMORY – MAPPED

FLAT-PLATE ANALYZER ARRAY

Figure 1.


HIGH VOLTAGE SUPPLY
ION TRAJECTORY
AMPLIFIER DISCRIMINATOR
TYPICAL FLAT PLATE
SAMPLE AND HOLD
V+
V-
DIGITAL TO ANALOG CONVERTER
TYPICAL
CONVERT
CHANNEL ADDRESS DECODER
DETECTOR PULSE COUNTER
COMMAND AND TELEMETRY INTERFACE
MSB'S 8-BIT COUNTER
LSB'S 8-BIT COUNTER
DATA
ADDRESS
CONTROL
RAM
PROM
μPROCESSOR
INTACK
INT
INTERRUPT CONTROLLER
CLOCK COUNTER
XTAL-CONTROLLED

The FPMA scan programs activate the digital to analog convertor and the array of sample and hold circuits in order to sustain the required voltages on the plates. The basis for these programs is the representation of the plate array in a memory array. There is a one-to-one map between a plate in the array and a location in memory. (See Figure 1.) The memory location, or locations, holds data representing the voltage to be placed on that plate and, if needed, other data. If we associate one byte (8 Bits) with each plate then we can encode 256 plate voltages via the digital to analog convertor. The FPMA scan programs thus read through this section of memory and output the plate voltages. A number of different programs could be accessed under telemetry command.

Activation of these programs would be under the control of a real time clock derived from a crystal oscillator. The clock output would periodically interrupt the microprocessor and initiate the program sequences required to accomplish the demanded functions.

The versatility and utility of this controller is dependent only upon the cleverness of the programmer. In addition, we would note that almost every point in the system is accessible to exercise by software. Thus, a controller diagnostic program can be written which will enable the controller to perform a number of self-tests.

THE INSTRUMENT DEVELOPMENT AND SUPPORT SYSTEM

In this section we provide a preliminary definition of the Instrument Development and Support System (IDSS). A list (see Table I) has been prepared of the uses of the IDSS in each of the three main phases of an experiment life cycle. These three phases are:

1) Instrument Development Phase

2) Instrument Fabrication, Calibration, and Test Phase (including field support)

3) Instrument Flight Phase

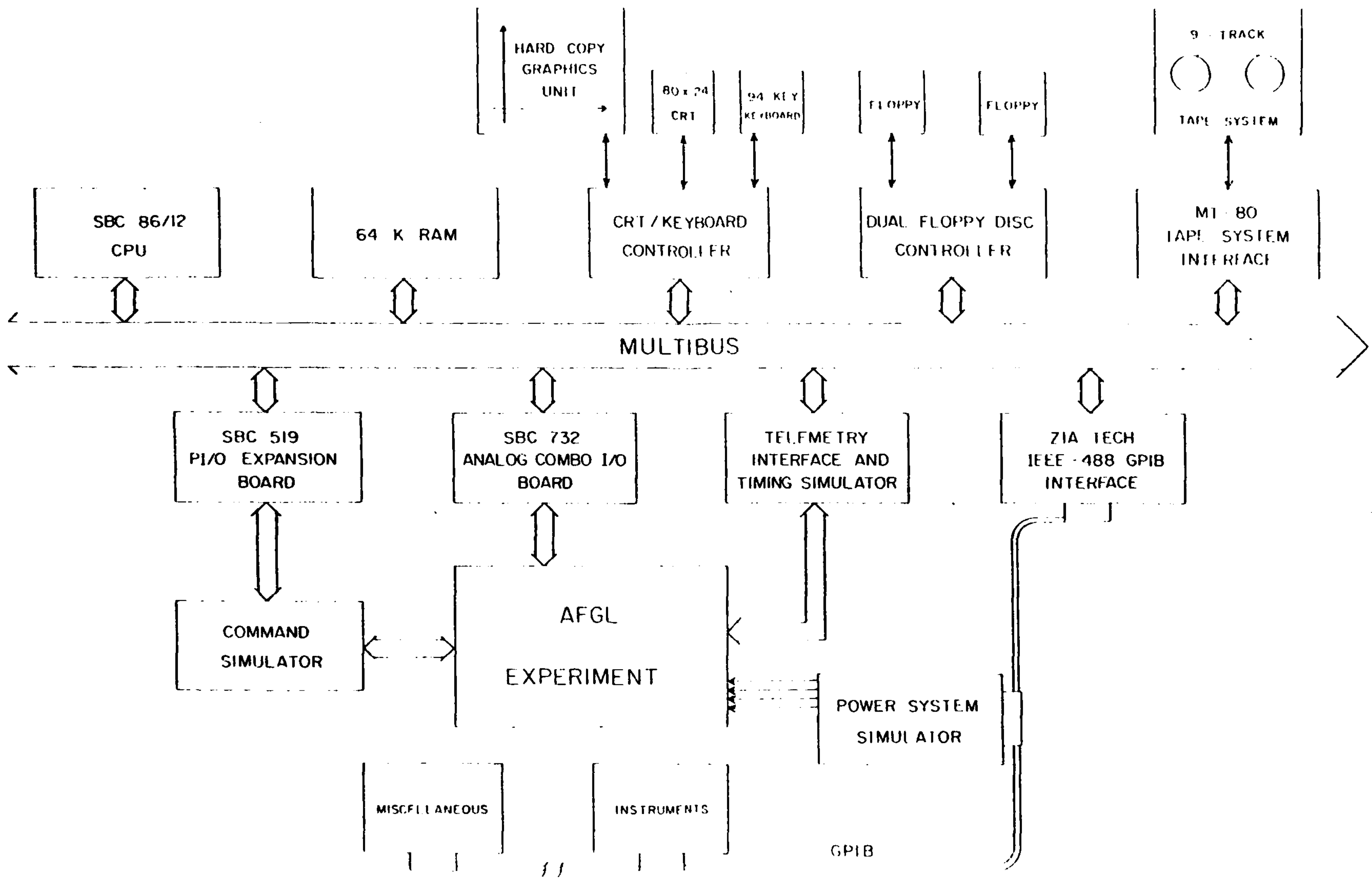
The IDSS is conceived as a microcomputer-based system dedicated to an instrument throughout its experiment life cycle. During the development phase the IDSS will be used to develop the microprocessor-based controller for the instrument and to perform a myriad of tests in an efficient and cost-effective way. The same IDSS grows naturally into the major support system for the calibration of the instrument. Routine testing procedures, documented as programs run by the microcomputer system, also become useful as field support, test, and checkout procedures. Ultimately, when the instrument is flown, the microcomputer system is dedicated to reduction of the telemetry data and preparation of tapes for analysis at a larger central computer center. The IDSS, of course, remains available for use in the laboratory facilities. This approach has been used with great success by the group at UCSD for their SCATHA experiment.

USE OF INSTRUMENT DEVELOPMENT AND SUPPORT SYSTEM

TABLE I

EXPERIMENT LIFE CYCLE

	INSTRUMENT DEVELOPMENT PHASE	INSTRUMENT FABRICATION, CALIBRATION AND TEST PHASE	INSTRUMENT FLIGHT PHASE
TECHNICAL	• Microprocessor Development System - Hardware - Software • Experiment Interface Simulator - Power System - Timing System - Command System - Telemetry System • Technical Data Recording and Presentation - Temperature Tests - Parameter Studies	• Calibration, Coordination and Control - Scan Particle Energy - Gather Data } DAS - Present Data } DAS - Record Data } DAS • First on Test - Power OK - Status OK - Command & Control OK • Field Stimulus Test - Stimulus on - Response Logged Checked against stds. • Extended Stimulus Test	• Telemetry Tape Data Reduction and Formatting • Preliminary Data Analysis • Data Presentation - Graphics Terminal - X-Y plots
MANAGEMENT	• Data Storage and Notebooks with Word Processing - Management Records - Activities Log - Dwgs List - Parts Lists - Task Assignments	CONTINUES THROUGHOUT	PROGRAM


HARD COPY GRAPHICS UNIT
80 x 24 CRT
94 KEY KEYBOARD
FLOPPY
FLOPPY
9 TRACK TAPE SYSTEM
SBC 86/12 CPU
64 K RAM
CRT / KEYBOARD CONTROLLER
DUAL FLOPPY DISC CONTROLLER
MT 80 TAPE SYSTEM INTERFACE
MULTIBUS
SBC 519 PI/O EXPANSION BOARD
SBC 732 ANALOG COMBO I/O BOARD
TELEMETRY INTERFACE AND TIMING SIMULATOR
ZIA TECH IEEE 488 GPIB INTERFACE
COMMAND SIMULATOR
AFGL EXPERIMENT
POWER SYSTEM SIMULATOR
MISCELLANEOUS
INSTRUMENTS
GPIB

The hardware from which the IDSS will be built is based upon the widely used MULTIBUS^{TM} standard computer interface. The bus structure provides a common element for communication between a wide variety of system modules which include: single board computers, memory and I/O expansion modules, peripherals and controllers. A system configuration suitable for use as an Instrument Development and Support System is shown in the enclosed Figure 1.

Standard, off-the-shelf modules are used wherever possible to implement the IDSS. These modules enable the processor to control and communicate with a variety of peripheral units, including a video terminal and keyboard, a pair of floppy discs, a printer, and a magnetic tape system suitable for producing IBM compatible magnetic tapes. The entire system is similar in concept to that used by the UCSD group to support their SCATHA instrument.

Specialized hardware is required for the instrument interface. In particular, we would want to implement a spacecraft command simulator, a power system simulator, and a telemetry interface and timing simulator. None of these interfaces is particularly complex, but each must be specified in some detail. This would be the main instrument dependent part of the IDSS.

The IEEE-488, General Purpose Interface Bus, is now being used widely to communicate between commercial instruments. By using a commercially available MULTIBUS to GPIB interface, we can communicate with these instruments. The system so configured is capable of a vast array of data acquisition, display, and control tasks. The versatility implication in such a system is absolutely essential to our conception of an Instrument Development and Support System.

MULTIBUS is a trademark of Intel Corporation.

The software requirements of the IDSS are not trivial. Nor should they be overestimated. In 1975 the Deputy Director for Research and Development of the Defense Department established a High-Order Language Working Group which issued a preliminary software specification, called Steelman. Several design cycles later, the effort has narrowed down to only one Pascal derivative dubbed ADA. This language is described in the Preliminary ADA Reference Manual, published as a SIGPLAN Notice (Vol. 14, No. 6, June 1979) by the ACM.

The closest thing to a standard Pascal available right now is the implementation designed by Prof. Kenneth Bowles and his team at the Institute for Information Systems at the University of California at San Diego . The UCSD-Pascal is available for use with the hardware we are proposing. A large pool of programmers familiar with Pascal is available at UCSD and thus we would plan to use Pascal for the development of the applications programs needed by the IDSS. As soon as the DOD finalizes the specification of ADA, we would then switch from Pascal to Ada -- an effort which should be reasonably efficient given the similarity of the two languages.

UCSD-Pascal is more than just a language. It is an entire system. Once installed on the hardware, one has immediately available a very useful set of programs. These include:

- Screen Oriented Editor - Basically this is an editor designed for use on the Video Display Terminal. For all practical purposes it implements a word processor which is extremely useful in writing and editing programs and in creating and modifying data storage and notebooks.

- Interactive Debugger - This routine causes conditional halts to be generated during program

compilation and is very helpful when writing programs in Pascal.

- Basic Compiler - For those who must, UCSD-Pascal provides a basic compiler.

- Linker and Assembler - The facilities exist for writing assembly language programs (for instance for special purpose I/O drivers).

- Utility Routines - A large number of utility routines are available which facilitate the use of the system.

Thus by installing UCSD-Pascal and by writing most of the applications programs in this language, we immediately obtain the following desired results.

- High probability of easy conversion to the DOD standard language Ada.

- A structured approach to program design since this is inherent in the language Pascal.

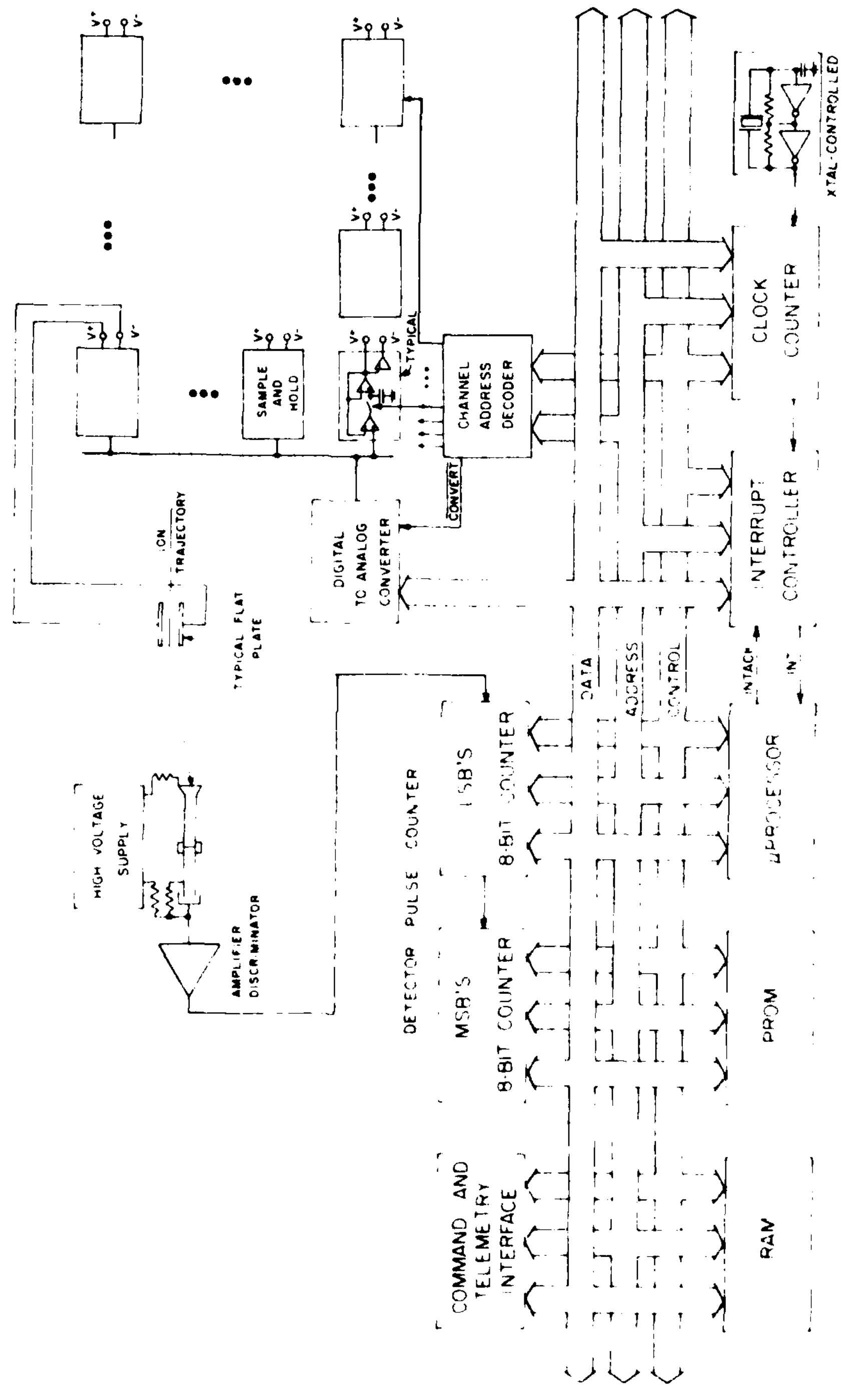
- An efficient high-level language for the writing of application programs.

Detailed testing would require use of the Instrument Development and Support System. Indeed, the IDSS will be based upon the Intel 8085 microprocessor, which since it will soon be available in CMOS, is a likely candidate for the instrument controller. Thus, programs designed for the controller can be tested on the IDSS and both the development and field testing procedures will be simplified.

The ongoing definition of the Instrument Development and Support System (IDSS) has focused on the specification of both hardware and software suitable for the application at hand. It is worthwhile to point out the general utility of the system for many uses.

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

In this report we have an innovative solution to the problem of low energy differential analyzers. The conceptual work must next be implemented and tested. We suggest that a modest implementation program be begun. This program would result in the fabrication of perhaps one dozen Flat Plate Microanalyzer Arrays. From these, one would be selected for use in an instrument which would be flown on a sounding rocket. A simple and cost-effective comparison of the FPMA with a more conventional analyzer could thus be performed. Such a program could probably be performed for less than $200,000 in a period of about one year.


SAMPLE AND HOLD
TYPICAL
CHANNEL ADDRESS DECODER
CONVERT
DIGITAL TO ANALOG CONVERTER
ION TRAJECTORY
TYPICAL FLAT PLATE
HIGH VOLTAGE SUPPLY
AMPLIFIER DISCRIMINATOR
DETECTOR PULSE COUNTER
8-BIT COUNTER
LSB'S
8-BIT COUNTER
MSB'S
COMMAND AND TELEMETRY INTERFACE
DATA
ADDRESS
CONTROL
CLOCK COUNTER
INTERRUPT CONTROLLER
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